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Assessing metal–semiconductor contact properties using *in situ*-biasing off-axis electron holography

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ABSTRACT

Characterizing metal–semiconductor contacts, particularly detecting Schottky barriers and distinguishing between ohmic and Schottky contacts, is essential for developing efficient semiconductor devices. Off-axis electron holography enables direct visualization of electrostatic potentials in a transmission electron microscope and has previously been used to study semiconductor *p–n* junctions under applied bias. Here, it is demonstrated that *in situ* biasing off-axis electron holography enables the direct characterization of the electrical properties of Schottky and ohmic metal–semiconductor contacts, including the visualization and quantification of Schottky depletion widths while simultaneously probing the behavior of the semiconductor *p–n* junction under operating conditions. To demonstrate this, Pt and W contacts with intentionally low and high contact resistance were deposited on GaAs *p–n* diodes using Ga-focused ion beam-induced deposition. The electrostatic potential across the metal–GaAs interface and *p–n* junction was mapped using electron holography under applied reverse bias. Electron holography successfully detected and quantified the Schottky depletion width *in situ* at the interface between W and p-GaAs and confirmed the ohmic behavior of the Pt contact to p-GaAs, demonstrating that electron holography can directly distinguish and characterize Schottky and ohmic contacts while simultaneously probing the behavior of the *p–n* junction. Thus, the results demonstrate its effectiveness for measuring nanoscale contacts in operating devices.

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I. INTRODUCTION

The nature of semiconductor–metal interfaces has important consequences that impact the functionality of microelectronic devices. Schottky contacts have a rectifying, diode-like behavior, while ohmic contacts provide a constant resistance regardless of the operating voltage regime. An ideal ohmic contact has a low-resistance as such a voltage drop across it is negligible compared to that across the active region of the device. Ohmic contacts are essential for the efficient operation of numerous devices including solar cells, transistors, and photodetectors. Therefore, the assessment of metal–semiconductor contact characteristics, specifically the detection of Schottky barriers, in operating devices is useful for device development.

In this paper, the changes in potential across the metal–semiconductor interfaces are measured using electron holography. Off-axis electron holography is an established transmission electron microscopy (TEM) technique for mapping the electrostatic potential at *p–n* junctions in semiconductor devices on a nanometer scale.[1–4] Electrically biasing the specimen inside the TEM during the holography analysis can also be used to track the response of the *p–n* junction, i.e., of the depletion width and the potential barrier.[5,6] However, previous *in situ* electron holography studies have focused primarily on semiconductor junctions, while the direct characterization of metal–semiconductor contact properties under applied bias has not yet been demonstrated. Electrical properties of the contacts have so far been inferred mainly from complementary *I–V* measurements rather than being directly analyzed by electron holography.[7] In this work, high-sensitivity off-axis electron holography with a sufficiently large field of view is used to directly characterize Schottky and ohmic metal–semiconductor contacts under applied bias while simultaneously

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TABLE I. Metal–semiconductor configurations present in the GaAs-W and GaAs-Pt *in situ* biasing specimen, with their predicted contact types (ohmic or Schottky), determined by comparing the work functions of the pure metals (ϕ_m) and the p- or n-doped GaAs (ϕ_s).

Metal/semiconductor	Junction configuration	Contact type
W/p-GaAs	$\phi_m < \phi_s$ 4.55 eV < 5.43 eV	Schottky
Pt/p-GaAs	$\phi_m > \phi_s$ 5.65 eV > 5.43 eV	Ohmic
W/n-GaAs	$\phi_m > \phi_s$ 4.55 eV > 4.03 eV	Schottky
Pt/n-GaAs	$\phi_m > \phi_s$ 5.65 eV > 4.03 eV	Schottky

probing the response of the semiconductor *p–n* junction in an operating device.

Similar to mapping the electrostatic potential across a semiconductor *p–n* junction, electron holography is just as well capable of detecting and mapping the changes in potential that arise from a depletion region on the semiconductor side of a Schottky metal–semiconductor interface. Thus, electron holography enables the identification of the contacts as ohmic or Schottky, and in the latter case, quantify the depletion width. Applying *in situ* electrical bias to the device during electron holography analysis also enables the study of contact characteristics and their behavior under operation-similar conditions while simultaneously allowing the response of the semiconductor *p–n* junction to be investigated. Thus, *in situ*-biasing electron holography enables comparative analysis of metal contacts between working devices and, hence, can provide important feedback for device fabrication.

The present study was conducted on a GaAs *p–n* homojunction with a symmetrical dopant concentration of 1×10^{18} cm^{-3}. *In situ*-biasing electron holography was used to analyze and compare two different metal–semiconductor interfaces fabricated on this identical GaAs *p–n* diode, a low-resistance and a high-resistance contact, i.e., a Schottky barrier.

II. THEORETICAL CALCULATIONS AND EXPERIMENTAL METHODS

A. Theoretical predictions of the GaAs-Pt and GaAs-W contact characteristics

Metal contacts with a lower and a higher resistance were created by depositing Pt and W to a GaAs *p–n* diode using Ga-ion beam-induced deposition (IBID) inside a dual-beam focused ion beam-scanning electron microscope (FIB-SEM). The FIB depositions were used here as a demonstration for the electron holography measurements of contact properties and do not compete with dedicated, pure metallizations realized under clean-room conditions. The choice of the deposited metals was made based on estimations of the junction characteristics of Pt and W to p-GaAs and n-GaAs by considering the work function differences of the contacting metal and semiconductor materials. For simplicity, a polycrystalline film of the pure metals was assumed. The work function of Pt is ϕ_m (Pt, polycrystalline) =5.65 eV[8,9] and of W ϕ_m (W, polycrystalline) =4.55 eV.[8,9] Certainly, the properties of the FIB-deposited metals will differ from these values due to the amorphous carbon content originating from the broken down precursor gases, the ion-beam-induced introduction of Ga impurities, as well as due to the changes in micro-structure of the IBID-metals compared to pure Pt and W.[10–14] The exact composition of the IBID depends on the Ga-ion beam energy and current, as well as on the area of the deposit. Due to the high amorphous C content in the deposition and the resulting change in the microstructure, the resistivity of the FIB-deposited metals is usually much higher than the expected values for the respective pure bulk metal. The resistivity of IBID-Pt deposited on a flat sample surface was reported to be 70–140 $\mu\Omega$ cm[15] and 10^3–10^5 times higher than that of bulk metallic Pt.[16] The resistivity of IBID-W layers was described to be around 200–250 $\mu\Omega$ cm,[10,17] while bulk W has a resistivity of 5.5 $\mu\Omega$ cm.[17]

As the work functions of FIB-deposited Pt and W are not well-documented, the values for the pure, crystalline metals were assumed in this discussion. The work function ϕ_s of a semiconductor is its Fermi level E_F measured with respect to vacuum level; hence, it is the sum of electron affinity χ and the conduction band edge E_{CB} relative to Fermi level, namely,

$$\phi_s = \chi + (E_{CB} - E_F). \tag{1}$$

In p-type semiconductor, the valence band edge E_{VB} is normally the reference. Therefore, the work function can be rewritten using the bandgap definition $E_g = E_{CB} - E_{VB}$; hence,

$$\phi_s = \chi + E_g - (E_F - E_{VB}). \tag{2}$$

GaAs has an energy bandgap of E_g(300 K) = 1.424 eV and an electron affinity χ = 4.07 eV.[18] The Fermi-level positions relative to the band edges are determined by the charge neutrality equation with the donor and acceptor concentration 1×10^{18} cm^{-3} for n-GaAs and p-GaAs specimen region, using NEXTNANO tool with parameters reported in Appendix A. Accordingly, Eqs. (1) and (2) yield the work functions ϕ_s (p-GaAs) =5.43 eV and ϕ_s (n-GaAs) =4.03 eV. The metal–semiconductor configurations for Pt and W, n-GaAs and p-GaAs are shown in Table I. For the given doping concentration of 1×10^{18} cm^{-3}, W is expected to form a Schottky contact with both n-GaAs and p-GaAs, whereas Pt will form a Schottky contact with n-GaAs but an ohmic contact with p-GaAs. Ohmic contacting of n-GaAs is generally more difficult due to its low work function compared to most standard metals.[8]

In order to assess the influence of the Schottky-type interfaces in the TEM lamellae on the resistive (or conductive) behavior of the *in situ*-biased specimen, the Schottky barrier height (ϕ_{SB}) as well as the built-in potential (V_{bi}) and the depletion width (W_d) on the semiconductor side of the contact interfaces were calculated,

$$\phi_{SB} = \phi_s - \phi_m, \tag{3}$$

$$V_{bi} = E_{VB} - \phi_m, \tag{4}$$

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TABLE II. Theoretically predicted properties of the Schottky contacts in the GaAs-W and GaAs-Pt specimens.

Metal/semiconductor	Schottky barrier height	Built-in potential	Depletion width
W/n-GaAs	$\phi_{SBn} = 0.50$ eV	$V_{bi,n} = 0.52$ eV	$W_d = x_n = 26.71$ nm
Pt/n-GaAs	$\phi_{SBn} = 1.60$ eV	$V_{bi,n} = 1.62$ eV	$W_d = x_n = 47.82$ nm
W/p-GaAs	$\phi_{SBp} = 0.93$ eV	$V_{bi,p} = 0.88$ eV	$W_d = x_p = 35.53$ nm

$$W_d = \sqrt{\frac{2\epsilon V_{bi}}{qN_a}}, \tag{5}$$

where ϵ is the dielectric constant of GaAs and q is the elementary charge. The above equations are for metal/p-GaAs, and similar equations are applied for metal/n-GaAs. Subsequently, the predicted values can be compared with the electrostatic potential measurements at the metal–semiconductor interface obtained via electron holography.

The parameters employed for the calculations are listed in Appendix A. The results are presented in Table II. It can be assumed that these values underestimate the actual Schottky barrier in the samples, as the resistance of the FIB-deposited metal contacts is likely to be considerably higher compared to the pure, polycrystalline metal assumed in the calculations. The values can, therefore, be comprehended as idealized reference values.

B. *In situ*-biasing TEM specimen preparation

For the *in situ* electron holography analysis of the metal–semiconductor contacts, specimens were prepared for examination in a Protochips Aduro holder on dedicated chips. The sample is a GaAs *p–n* structure grown by molecular beam epitaxy and comprises a 1 μm-thick Be-doped (p-type) layer grown on a 1 μm-thick Si-doped (n-type) layer on a n-doped GaAs (0 0 1) substrate. Two electron-transparent parallel-sided cross sections were prepared from the bulk GaAs sample by Ga-FIB milling using a FEI Strata 400. The procedure is described in Figs. 1(a)–1(h). The lamellae were cut parallel to the crystallographic [1$\bar{1}$0] direction so that the TEM viewing direction is along the [110] zone axis. The specimens were lifted out from the bulk wafer [Fig. 1(c)] and were deposited on MEMS chips (Protochips) to enable *in situ*-biasing inside the TEM [Figs. 1(d) and 1(e)]. The semiconductor lamellae were electrically connected to the MEMS chips using IBID [Fig. 1(f)]. One lamella was contacted with IBID-W and one with IBID-Pt, using organometallic gas injection system (GIS) precursor gases, namely, tungsten hexacarbonyl [$W(CO)_6$] and methylcyclopentadienyl platinum trimethyl ($C_9H_{16}Pt$), respectively. The specimens were made electrically functional in two key steps. First, the bottom side of the lamellae were cut [Fig. 1(g)] to reduce the amorphous damage and re-deposition occurring during the lamella lift-out, thus reducing surface currents during biasing. Second, the current circuit in the specimens were edited by introducing isolation cuts. To force the charge carriers to pass through the *p–n* junction during biasing, one isolation was cut from the bottom, through the semiconductor specimen into the top metal layer [Fig. 1(g)], while a second isolation was milled through the top metal layer into the semiconductor substrate [Fig. 1(h)]. The lamellae were thinned down progressively to electron-transparent thicknesses operating the FIB at 16 kV. In the last preparation step, the surfaces of the lamellae are polished at 2 kV and 0.15 nA to reduce amorphous surface damage.

The electrical circuit, along with the cut geometry of the *in situ* biasing lamella, is illustrated in Figs. 1(i) and 1(j). The *p–n* diode is connected in series with the resistances of the substrate and the top and bottom metal contacts, while the surface resistance is connected in parallel.

C. Off-axis electron holography

Electron holography uses a parallel electron wave to illuminate the specimen and an adjacent vacuum region. The electrostatic potential changes in the semiconductor specimen cause phase changes of the electron wave passing through the specimen. Interference of this object wave with a reference wave passing through vacuum yields an electron interference pattern (hologram), from which the electron phase shift and amplitude can be reconstructed by using a simple Fourier reconstruction procedure. In the absence of magnetic fields and dynamical diffraction effects, this phase shift is directly proportional to the projected electrostatic potential distribution inside the specimen via

$$\Phi = C_E \int_0^t (V_{dopant} + V_{MIP}) dz, \tag{6}$$

where the total measured potential is composed of V_{dopant}, the electrostatic potential related to active dopants in the semiconductor, and V_{MIP}, the volume-averaged mean inner potential of the undoped semiconductor material. C_E is an interaction constant determined by the acceleration voltage of the incident electron beam ($C_E = 0.0073$ rad nm^{-1} V^{-1} for 200 kV electrons) and t is the TEM specimen thickness.

The hologram acquisitions on the GaAs-W and GaAs-Pt specimens were performed on the regions indicated in the overview images in Figs. 2(a) and 3(a). Intentionally, thick regions were examined. The crystalline thicknesses, $t_{crystalline}$, were measured to be 450 ± 17 nm for GaAs-W and 370 ± 10 nm for GaAs-Pt using STEM two-beam convergent beam electron diffraction (CBED). As evident from Figs. 2(a) and 3(a), IBID-W (or Pt) serves as electrical top and back contact of the respective GaAs lamella to the metal tracks of the chip. The specimen support chip is mounted in the Protochips Aduro 500 biasing TEM specimen holder, where the chip metal tracks can be contacted individually. *In situ*-biasing of the samples was performed using a Keithley power supply connected to the TEM holder. The electron holography experiments were performed in a double-corrected FEI Titan

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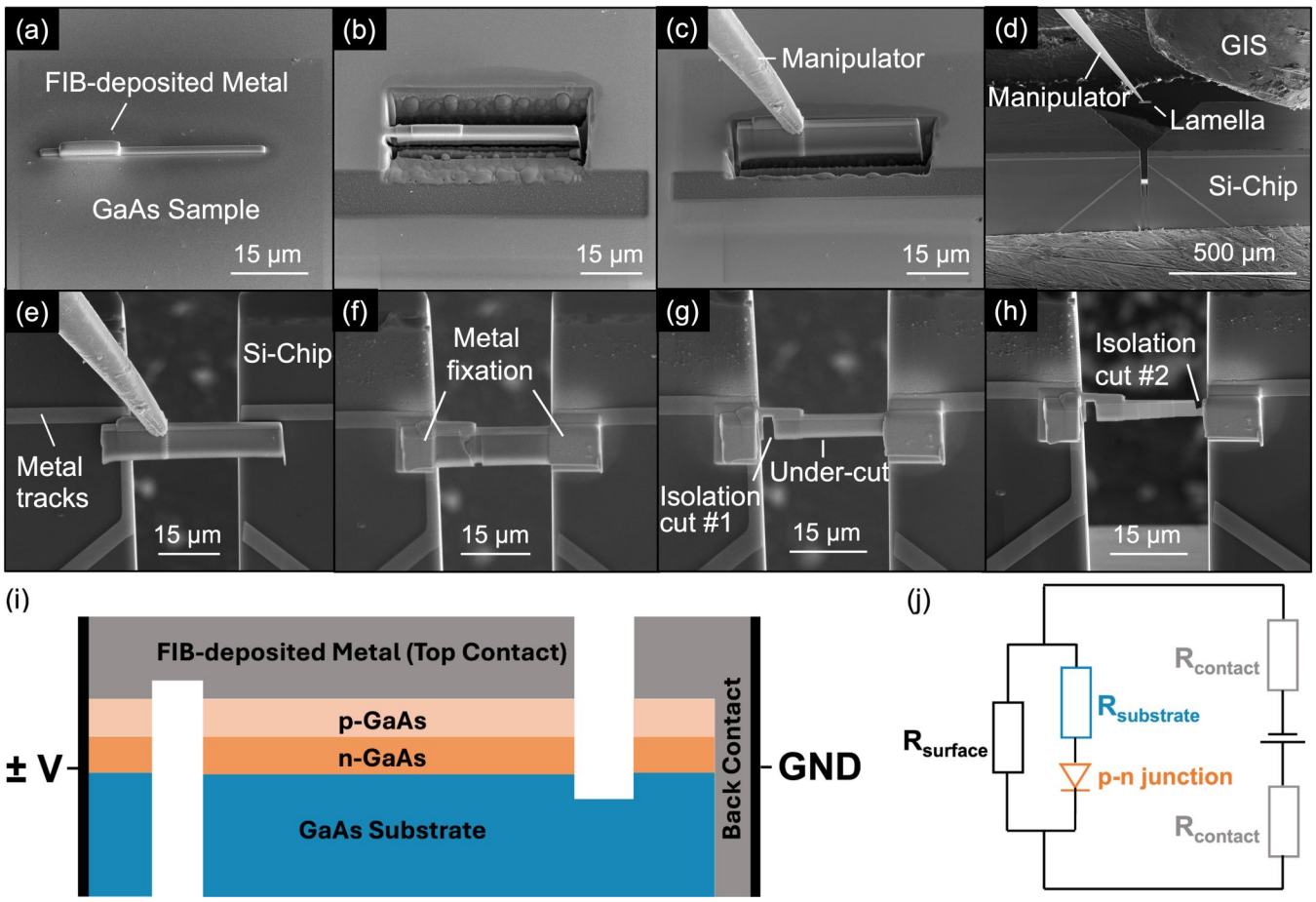


FIG. 1. Preparation procedure of a TEM lamella on a chip for *in situ* biasing TEM analysis. (a) Ion-beam- induced metal (W or Pt) deposition (IBID) for protection and electrical contacting. (b) By milling side-trenches and performing an L-cut, a free-standing lamella is shaped. (c) The lamella is welded to a manipulator by IBID of W and the last side-connection is cut free to allow the lamella lift-out. (d) The lamella is transferred to the Si-half MEMS chip, where it is positioned on the chip trench as shown in (e). (f) Each lamella side is electrically connected to the respective metal tracks by large ion-beam-induced metal depositions. (g) The lamella sidewalls are cleaned and damage at the bottom edge is removed by an undercut, and the first isolation is cut for circuit editing. (h) After shaping and thinning the lamella to the desired thickness, the second isolation cut is milled. The preparation is finished off by ion-polishing each side at 2 kV. All secondary electron SEM images were acquired at 5 kV and 0.40 nA. (i) Schematic of the TEM lamella geometry designed for *in situ* biasing experiments and (j) the corresponding electrical circuit within the lamella.

Ultimate operated at 200 kV. The electrical bias was applied to the top metal contact of the samples due to its proximity to the studied metal–semiconductor interface and the GaAs *p–n* junction. The back contact was connected to ground (GND). A positive voltage (+V) is applied to the p-side of the GaAs junction, which leads to forward biasing of the junction, while a negative voltage (−V) corresponds to reverse biasing.

Acquisitions were taken for different applied reverse voltages in the range of −3 to 0 V in steps of 1 V using the acquisition parameters listed in Appendix B (Table III). To ensure a high phase sensitivity, stacks of 30 electron holograms were acquired for 8 s each on a 4k Gatan Oneview camera. To prevent the specimen from over-heating, the current flowing through the junction was limited to 100 μA by setting the compliance current in the Aduro Software. Using low-magnification electron holography settings—achieved by adjusting the diffraction lens excitation—allowed us to fit the specimen *p–n* junction, the metal–semiconductor interface and the vacuum reference region above it within the image field of view (FOV). The phase information was reconstructed from the hologram stacks using HOLOVIEW, an internal software written at CEA LETI Grenoble.

For electrical analysis of semiconductor devices and their *in situ*-biasing within the TEM, preserving the sample's electrical properties during FIB preparation of electron-transparent slices is critical. High-energy Ga-ion milling alters the surface of semiconductor specimens, impacting their electrical performance. First, an amorphous surface layer is formed, which contains a high concentration of implanted Ga-ions, thus creating a conductive path

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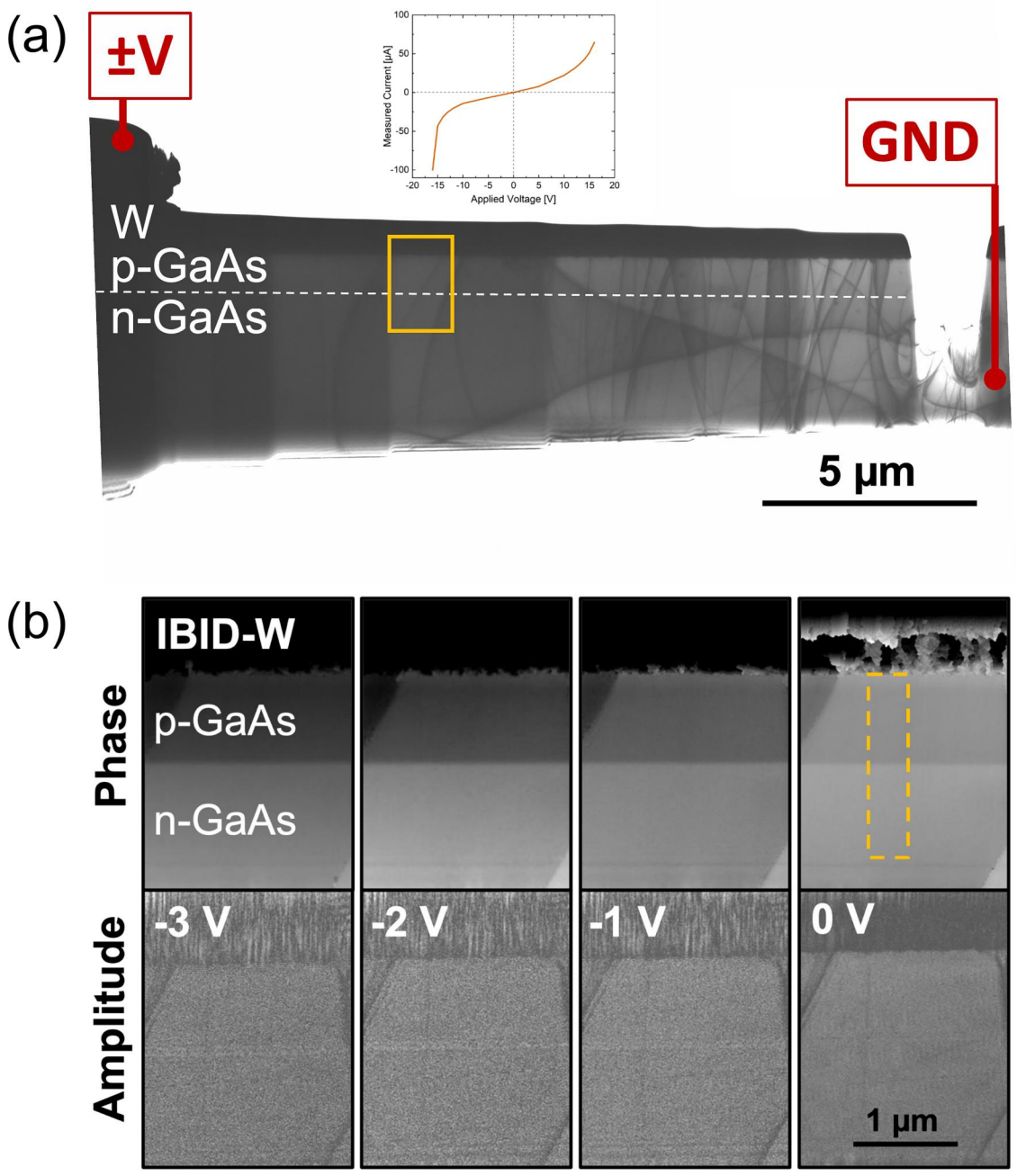


FIG. 2. (a) Low-magnification TEM image of the GaAs-W specimen attached to the biasing chip. The positions of the electrical bias (±*V*) and ground (GND) connectors are marked in red. The region examined by *in situ* biasing hologram acquisitions is highlighted in orange, and the GaAs *p*–*n* junction is indicated by the white dashed line. The insert shows the *I*–*V* characteristics of the GaAs-W lamella. (b) Phase and amplitude images of the *p*–*n* junction at 0 V and selected applied reverse biases. Phase profiles are extracted from the dashed region.

during *in situ*-biasing. This can result in short circuits for the current during the *in situ*-biasing experiment. To ensure successful biasing, it is crucial to minimize this leakage current to prevent the specimen from excessively drawing current, which could damage or cause failure of the diode. The reduced parallel surface resistance decreases the overall resistance of the system, thus increasing the total current. However, it does not affect the amount of potential which is dropped across the *p*–*n* junction diode.

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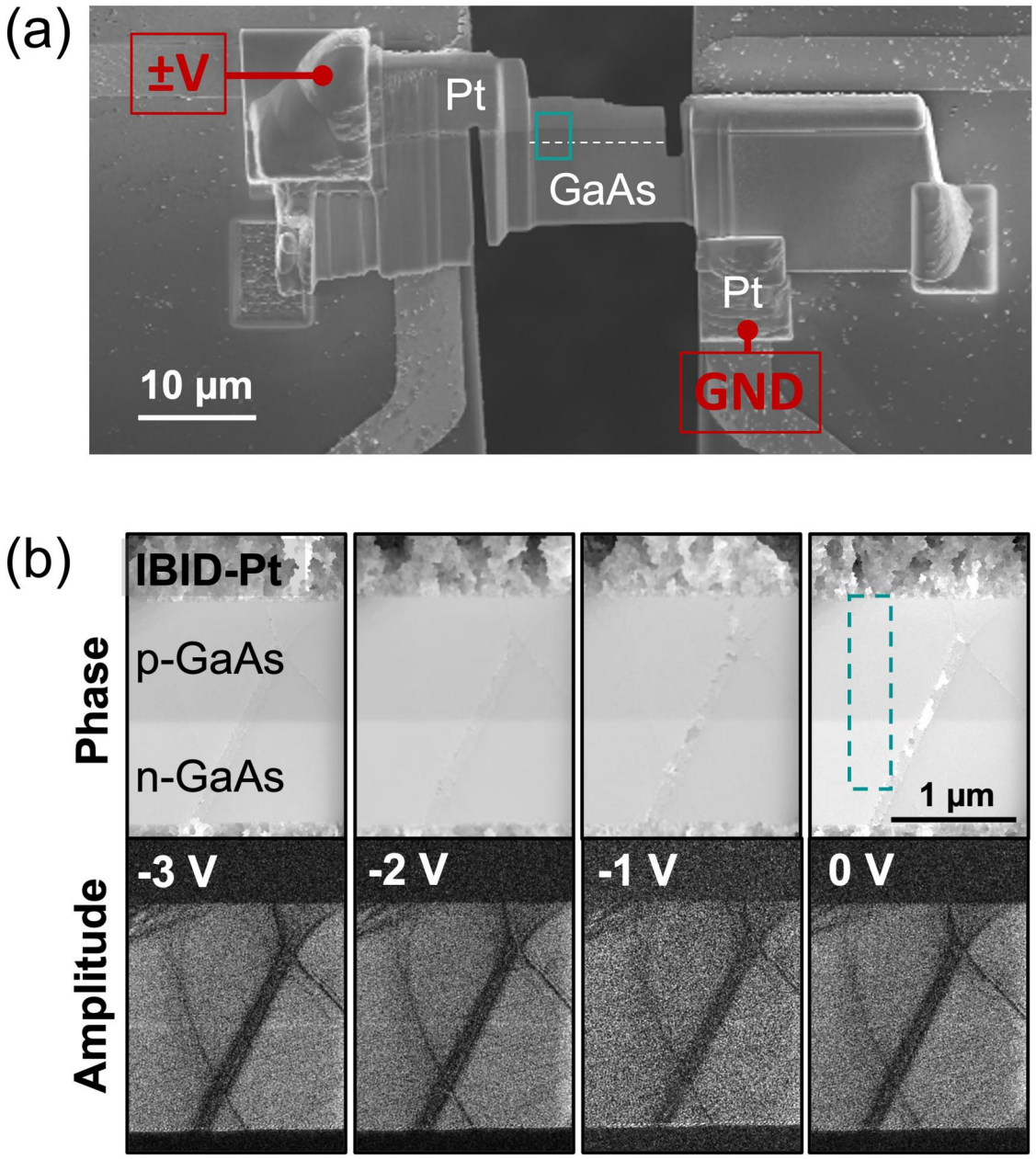


FIG. 3. (a) Secondary electron SEM image of the GaAs-Pt specimen attached to the biasing chip. The positions of the electrical bias (±*V*) and ground (GND) connectors are marked in red. The region examined by *in situ* biasing hologram acquisitions is highlighted in turquoise, and the GaAs *p–n* junction is indicated by the white dashed line. (b) Phase and amplitude images of the *p–n* junction at 0 V and selected applied reverse biases. Phase profiles are extracted from the dashed region.

Below the amorphous surface layer, an electrically damaged (simplified as the so-called inactive layer), yet still crystalline, subsurface layer is formed due to the collision cascade induced by the Ga-ions. This crystalline region, while retaining its structure, contains point defects (vacancies, interstitials, and impurities) negatively impacting the doping activity of the semiconductor.[19–21] The surface defect states pin the Fermi level, which leads to surface band bending. Hence, a surface-near depletion region is formed, which reduces the absolute built-in potential across a junction measured by electron holography, thus complicating

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quantification.[20,22,22–26] Therefore, to mitigate the influence of the electrically inactive surfaces, the FIB-lamellae in this study were prepared deliberately thick. The surface damage was further significantly reduced by using a low ion beam energy and current, along with a low incidence angle of the Ga-ion beam, for the preparation of the GaAs-W and GaAs-Pt specimens.

For a meaningful quantification of the electrostatic potential from the measured phase shift using Eq. (6), the electrically inactive surface layer must be measured, and only the electrically active specimen thickness should be employed in the potential calculation. Assuming that this thickness is constant across the specimen, the measured phase across a *p–n* junction can then be expressed as

$$\Phi = C_E V_{total}(t_{crystalline} - t_{inactive}), \tag{7}$$

where $t_{crystalline} - t_{inactive}$ yield the electrically active thickness t_{active}. The procedure employed for estimating the inactive thickness is detailed in Appendix C. For the GaAs-W sample, it was measured as 151 ± 23 nm in total, corresponding to about 75.5 nm on each lamella surface, which do not contribute to the total built-in junction potential. This value is close to the 172 ± 15 nm inactive thickness reported by Cooper *et al.*[27] for a GaAs *p–n* junction specimen with the same symmetrical doping concentration of 1×10^{18} cm^{-3}, prepared using the same FIB operating voltage of 16 kV. Sasaki *et al.* measure an inactive layer of about 120 nm for 1×10^{18} cm^{-3} doped GaAs.[20] Anada *et al.* reported a larger value of 202 ± 10 nm, although using a GaAs specimen with a higher doping concentration (1×10^{19} cm^{-3}).[28] In addition to doping concentration, variations in FIB preparation conditions (Ga-ion beam energy, current, and milling angle) and differences in evaluation methodology may contribute to the discrepancies among the reported values.

When the electrically inactive thickness of 151 ± 23 nm is taken into account in the simulation of the expected phase shifts for the remaining active thicknesses in the GaAs-W sample, the measured phase shifts are very close to the expected values (see Appendix C). The same electrically inactive thickness was used to quantify the electrostatic potential from the measured phase distribution in both the GaAs-W and GaAs-Pt specimens. This is justified by several factors that ensure methodological consistency: Both specimens were extracted from the exact same GaAs *p–n* junction wafer, guaranteeing identical bulk doping concentrations and eliminating composition-related variability as a source of systematic error. Furthermore, the same preparation protocol was applied throughout, with identical Ga-ion beam energy, currents, and milling angles employed during each fabrication step.

III. RESULTS AND DISCUSSION

The reconstructed phase and amplitude images of the GaAs-W and GaAs-Pt specimens, acquired at 0 V and under reverse bias up to −3 V, are displayed in Figs. 2 and 3, respectively. A key factor for electron holography analysis is to minimize the dynamical diffraction by tilting the specimen off the zone axis to a weakly diffracting orientation. Here, the specimens were tilted away from the [110] zone axis along the (001) interface of the GaAs *p–n* structure to avoid information loss due to projection and broadening of the *p–n* junction. In the thicker regions, as they were used in this study to minimize surface effects for the potential measurement, the diffraction contrast cannot be entirely removed. This is because, during sample preparation for *in situ* biasing, the long lamella needs to be attached on both ends, which will introduce bending, leading to bend contours and intensified dynamical diffraction in the holograms, visible in the amplitude images in Figs. 2(b) and 3(b). For reliable phase interpretation, the contrast in the amplitude images must be homogeneous. The regions examined were selected accordingly, as indicated in Figs. 2(b) and 3(b). Phase profiles were extracted from these regions beginning at the metal/p-GaAs interface and extending across the *p–n* junction, averaging across a 200 nm region. The electrostatic potential was calculated using Eq. (7) employing the electrically active thickness of the respective regions: $t_{active} = 299 \pm 23$ for GaAs-W and $t_{active} = 205 \pm 23$ for GaAs-Pt. The resulting potential distributions are shown in Fig. 4.

The contact properties differ markedly between the two specimen. The GaAs-W specimen exhibits a pronounced increase of the measured potential toward the metal, indicating the depletion region of the Schottky contact. This depletion region is also clearly visible in the phase images [Fig. 2(b)] as a bright phase contrast along the W/p-GaAs interface. As the metal work function (ϕ_m) is lower than that of the p-type semiconductor (ϕ_s), electrons flow from the IBID-W metal into the p-GaAs, forcing the semiconductor bands to bend upward until the Fermi levels of metal and semiconductor align. In this equilibrium state, the p-GaAs region adjacent to the interface is depleted of holes, creating a potential barrier that impedes majority-hole transport to the contact, as illustrated in Fig. 4(c). The holography measurements, therefore, show an upward trend of the electrostatic potential toward the W/p-GaAs interface [Fig. 4(a)]. In contrast, at the Pt/p-GaAs interface, the profiles suggest a decreasing potential toward the metal, which is characteristic of an ohmic contact to a p-type semiconductor. As the metal work function (ϕ_m) exceeds that of the semiconductor (ϕ_s), holes flow from the IBID-Pt into the p-GaAs until the Fermi levels align. This hole injection produces an accumulation on the semiconductor side of the interface [illustrated in Fig. 4(d)], leading to a slightly more negative phase contrast (i.e., a lower electrostatic potential) in the vicinity of the p-GaAs surface [Fig. 4(b)].

The electron holography analysis, thus, confirms that the FIB-deposited Pt layer forms an ohmic contact to p-GaAs, whereas the FIB-deposited W layer forms a Schottky contact to the same p-GaAs. The IBID-W/n-GaAs bottom contact lies outside the of the holography experiment; nevertheless, its Schottky character is evident from the *I–V* curve of the GaAs-W sample shown in Fig. 2(a). The double Schottky contacts induce the characteristic symmetric *I–V* response. The interpretation of the *I–V* curve with respect to the potential drop at the *p–n* junction is, however, not straightforward, as the metal contacts fundamentally control and influence the measured characteristics of the entire system. The cut-in voltage, where the GaAs *p–n* junction begins to conduct, should be close to the GaAs bandgap energy of 1.42 V.

The step in potential measured across the depletion region at the contact interface is 0.85 V, which is similar to the

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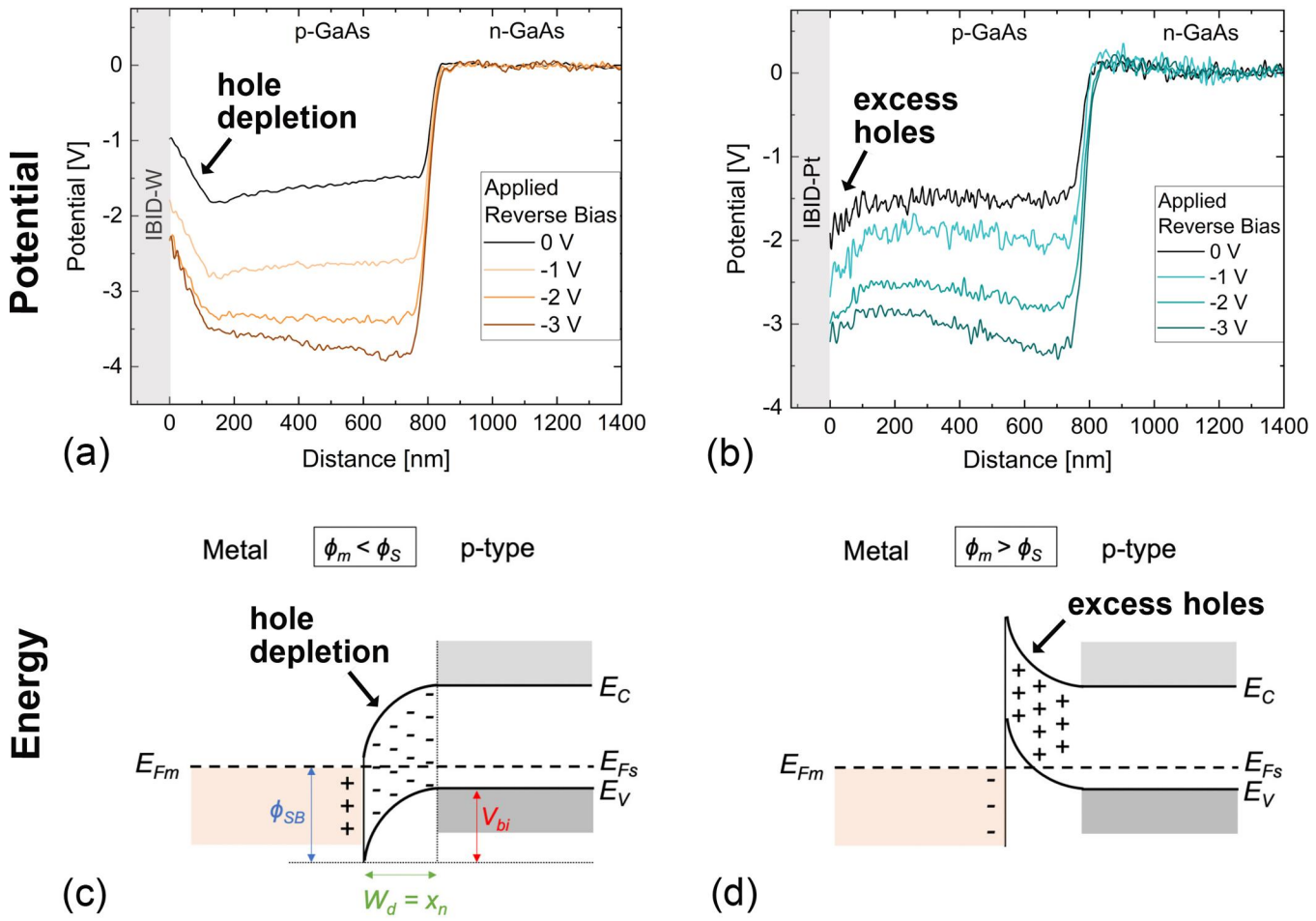


FIG. 4. Potential distributions measured as a function of the applied reverse biases starting from the metal/p-GaAs interface and extending across the GaAs *p–n* junction in (a) the GaAs-W specimen at $t_{active} = 299 \pm 23$ nm and (b) the GaAs-Pt specimen at $t_{active} = 205 \pm 23$ nm. (c) and (d) Schematic energy band diagrams illustrating the two metal–semiconductor configurations. For the Schottky contact in (a), a depletion region of width W_d forms on the semiconductor side, and majority carriers encounter a potential barrier of height V_{bi} at the interface. The barrier for electrons in the metal is the Schottky barrier, ϕ_{SB}. In contrast, for ohmic contacts as in (b), no depletion region forms, and majority carriers face no potential barrier at the interface.

simulated value of 0.88 V (see Table II). The width of the Schottky depletion region at the contact interface, measured from the derivative of the potential distribution under zero applied bias, is 133 nm. From the measured W_d and V_{bi} of the Schottky contact depletion region, the N_a in the p-GaAs layer was calculated as $6.9 \times 10^{16}\,\mathrm{cm}^{-3}$, which is lower than the expected $10^{18}\,\mathrm{cm}^{-3}$ (Appendix A). The large measured depletion width, and the related underestimation of N_a, can be largely explained by the fact that the W/p-GaAs interface is not a pure Schottky contact, which is assumed in the simulations (see Table II for the estimation of Schottky characteristics). Instead, the real specimen is a more complex system due to the presence of the GaAs *p–n* junction and the W/n-GaAs Schottky rear-contact. The complexity of the electrical specimen circuit is evident from the *I–V* characteristics (Fig. 2). The extended width of the contact depletion region in the specimen and the related underestimation of N_a could, hence, be caused by the electrostatic redistribution of holes inside the p-GaAs, which is a consequence of the voltage drop across the GaAs *p–n* junction.

The experimentally measured depletion width is considerably larger than the simulated value of 35.53 nm for pure W (Table II). This discrepancy was expected as the calculation served solely the purpose to provide a minimum reference value to put the measured values into context. The fact that the IBID-W/p-GaAs contact displays a wider depletion region than theoretically predicted can be primarily attributed to the fact that the W metal deposition deviates from the assumed pure and ideal contact. The related factors that contribute to the increased contact resistance are the following:

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- First, and most importantly, the FIB-deposited metal layers are not pure in composition. They contain C and Ga impurities and exhibit microstructural deviations. For instance, the Ga-doped W–C layers are typically amorphous,[10,11] while the IBID-Pt forms micrometer-sized Pt grain networks embedded within a Ga-doped amorphous C matrix.[12–14] As elaborated in Sec. II, these compositional and microstructural differences lead to higher contact resistances compared to the pure metals and, thus, explain largely the larger measured depletion width for the W/p-GaAs Schottky contact.
- Second, the deposition of metal contacts on GaAs is inherently challenging due to several factors. GaAs surfaces are highly prone to As loss,[29,30] and the high volatility of As often necessitates the use of a diffusion barrier layer (e.g., Ni)[31,32] prior to contact deposition to preserve the surface integrity. Furthermore, III–V semiconductors such as GaAs are particularly susceptible to Fermi-level pinning caused by surface defect states. These defect states are introduced by the Ga-ion milling during FIB processing as well as by the metal deposition process itself.
- Third, the quality of the metal contacts deposited via FIB is likely compromised by the less-than-ideal cleanliness of the deposition environment. Despite plasma cleaning of the semiconductor wafers prior to FIB processing, the transition from the plasma cleaner to the FIB chamber occurs under ambient air, which exposes the surface to potential contamination. Additionally, the FIB-SEM chamber itself is not a clean environment. Addressing this challenge will require the use of ultrahigh vacuum FIB-SEM systems and clean transfer mechanisms for bulk specimen loading, which would ensure better control over surface cleanliness during future contact deposition processes.

The first factor primarily explains the large discrepancy between predicted and experimental depletion widths in the W/p-GaAs contact. The second and third factors are minor contributors, accounting for why FIB-deposited metal contacts generally show higher resistance than theoretical predictions.

Beyond simplified assumptions about W metal deposition, the broader-than-predicted depletion region in the IBID-W/p-GaAs contact also reflects inherent simplifications in the theoretical models themselves. These models are typically based on idealized metal–semiconductor interfaces and, therefore, do not fully capture the complexities of the real specimens. Specifically, the Schottky contact characteristics were calculated for a bulk p-GaAs semiconductor and do not consider incomplete dopant ionization or interface and surface phenomena in the electron-transparent TEM lamella, such as surface Fermi-level pinning and associated band bending.

The deviation of the experimental values from the simulated contact properties was expected. Nevertheless, the fundamental distinction between the ohmic IBID-Pt/p-GaAs contact and the Schottky IBID-W/p-GaAs contact remains intact, and electron holography enables to clearly distinguish the two contact natures.

The objective was to analyze the Schottky contact under applied bias to study its influence on the behavior of the GaAs *p–n* junction during biasing. Figures 4(a) and 4(b) show the effect of the reverse-applied bias on the IBID-W/p-GaAs and IBID-Pt/p-GaAs contact characteristics. The potential distribution in the p-GaAs adjacent to the IBID-Pt contact remains unchanged, as expected for an ohmic contact. However, the IBID-W/p-GaAs Schottky contact does not exhibit any significant changes in phase step or in depletion width within the applied bias range from 0 to −3 V either.

Still, the observed response of the GaAs *p–n* junctions to the applied reverse bias clearly confirms the functional biasing of the two specimens. Figure 5 shows (a) and (b) the response of the electric field distribution, (c) the derived depletion width, and (d) the step in potential across the GaAs *p–n* junctions as a function of applied bias for both specimens, GaAs-W and GaAs-Pt. The electric field distributions in Figs. 5(a) and 5(b) show clearly the expected widening of the *p–n* depletion region with increasing reverse bias. The depletion widths are quantified from these profiles as the distance between the x-intercepts of the linear extrapolations of the peak edges to the x-axis. The results for both specimens are plotted in Fig. 5(c) as a function of the applied bias in comparison to the depletion width expected from NEXTNANO simulations of the present GaAs structure. The depletion widths measured for both *p–n* junctions without applied bias (at 0 V) agree within in the error: 82 ± 1 nm in GaAs-Pt and 81 ± 1 nm in GaAs-W. This demonstrates that using electron holography the junction depletion width can be reproducibly measured across different TEM lamellae, prepared from the same bulk specimen using a careful and consistent preparation scheme. The experimental values at 0 V are higher than the depletion width of 62 nm estimated from simulations. This difference can be primarily ascribed to the lower abruptness of the actual *p–n* junction as well as the inclusion of partially depleted transition regions in the measured depletion width. The overall observed trend of the depletion width with applied voltage meets the expectations, as it significantly increases under reverse bias. The anticipated reduction of W_d with forward bias is more pronounced in the GaAs-Pt specimen, although it is also slightly noticeable in the GaAs-W sample.

Figure 5(d) shows the step in potential ΔV_{n-p} at different applied biases is quantified from the phase step $\Delta\Phi_{n-p}$ using Eq. (7), accounting for the estimated electrically inactive surface thickness ($t_{inactive}$). When accounting for $t_{inactive}$, at 0 V applied bias the measured built-in potential of the GaAs specimen *p–n* junction, 1.37 ± 0.1 V in GaAs-Pt and 1.42 ± 0.1 V in GaAs-W, is similar to the 1.41 V expected from the simulations. The slightly higher deviation for the GaAs-Pt sample can be explained by the fact that the assumed $t_{inactive}$ was not specifically measured for this specimen, as it does not have a sufficient number of different thicknesses to derive the inactive thickness.

With applied bias, the behavior of the step in potential across the *p–n* junction is generally as expected, i.e., it is increasing with reverse bias, while it slightly decreases with forward bias. If the entire applied bias would be dropped across the *p–n* junction, the step in potential at the junction in the equilibrium state (without applied bias) should be increasing by the magnitude of the applied reverse voltage. For example, at a reverse bias of −2 V, ΔV_{n-p} would be increasing from 1.41 V at 0 V to 3.41 V. However, the measured values are 2.58 V in GaAs-Pt and 2.98 V in GaAs-W. Hence, only 1.21 and 1.56 V of the 2 V applied voltage are dropped across the *p–n* junction in the GaAs-Pt and GaAs-W,

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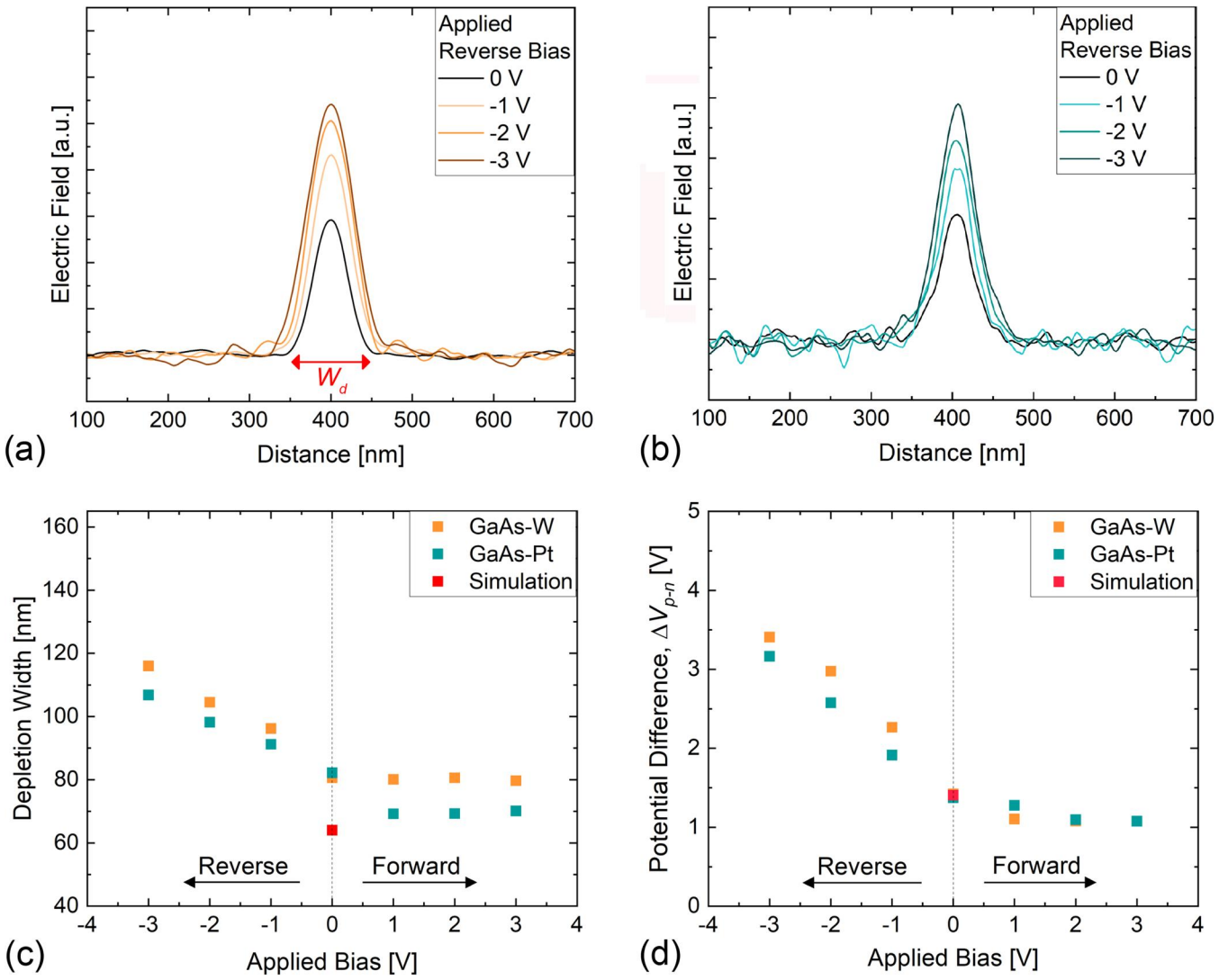


FIG. 5. Electric field distribution across the *p–n* junction in the (a) GaAs-W specimen at $t_{crystalline}$ =450 ± 17 nm and (b) the GaAs-Pt specimen at $t_{crystalline}$ =370 ± 10 nm. The profiles were derived from the experimental potential profiles using the first differential. (c) Width of the *p–n* depletion region (W_d) as a function of the applied voltage, measured from the electrical field profiles in (a) and (b). The expected values for the ideal junction (abrupt and complete ionization) under reverse bias, derived from the NEXTNANO simulation of the GaAs specimen, are shown for comparison. (d) Step in potential across the *p–n* junctions as a function of applied voltage.

respectively. While still the largest share of the applied bias is dropped across the *p–n* junctions, a small part is dropped elsewhere in the system, thus reducing the amount of voltage dropped across the junction.

A notable result of the *in situ* biasing experiment is, however, the weak variation of the potential step and depletion profile at the W/p-GaAs interface, despite the substantial change in the externally applied voltage. This is because the W/p-GaAs contact, the p-GaAs layer, and the *p–n* junction are series-connected, and the applied voltage is partitioned among the different resistances, dropping mainly across the GaAs *p–n* junction and partly across the p-GaAs region (see Appendix D). Only a small fraction of the reverse voltage is dropped at the metal–semiconductor interface, so the metal's Fermi level shifts only marginally. Consequently, the depletion region on the semiconductor side of the IBID-W/p-GaAs contact remains essentially unchanged under reverse bias.

IV. CONCLUSION

This work demonstrates how TEM off-axis electron holography measurements can be used to determine the nature of metal–semiconductor contacts, effectively distinguishing between ohmic

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and Schottky behaviors in operating devices. From a GaAs p–n junction, two specimens were cut and contacted using Pt and W ion-beam deposition. Theoretical calculations predicted an ohmic contact of Pt to p-GaAs and a Schottky contact of W to p-GaAs. The electrostatic potential distribution measured at the metal/p-GaAs interfaces confirmed that Pt forms an ohmic contact, while W creates a Schottky barrier, characterized by a measurable depletion region of 133 nm and a related step in potential of 0.85 V. Holography analysis of the two specimens under *in situ* applied bias clearly showed the influence of the contacts on the behavior of the GaAs p–n junction during biasing. The step in potential and the depletion width of the p–n junction were clearly increasing with applied reverse bias, showing that the applied voltage is mostly dropped across the p–n junction, thus confirming functional biasing. The double Schottky contacts of the GaAs-W specimen, W/n-GaAs and W/p-GaAs, and the Schottky Pt/n-GaAs back contact of the GaAs-Pt specimen account for the remaining voltage drop. The constant depletion width and the potential step measured across the W/p-GaAs Schottky contact under applied bias were attributed to the predominant voltage drop occurring across the p–n junction and the corresponding redistribution of charges within the p-GaAs layer. Therefore, *in situ*-biasing electron holography proved useful in identifying the fundamental metal–semiconductor contact characteristics and providing deeper insights into the operation of functional semiconductor circuits.

In practical semiconductor device engineering and reliability studies, applying quantitative *in situ* mapping of electrostatic potentials at metal–semiconductor interfaces can provide a means to investigate contact degradation and processing-induced defects that affect device performance. The compatibility with applied bias may further allow for the study of dynamic phenomena in operational devices, such as breakdown mechanisms and charge redistribution under load. As device dimensions continue to shrink and interfacial effects increasingly govern overall behavior, electron holography has the potential to become a valuable technique for validating contact designs, optimizing fabrication processes, and diagnosing performance-limiting defects.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

Vita Mergner: Formal analysis (lead); Investigation (lead); Methodology (lead); Writing – original draft (lead); Writing – review & editing (equal). **Jing Li:** Writing – review & editing (supporting). **Rafal E. Dunin-Borkowski:** Funding acquisition (lead); Supervision (equal). **David Cooper:** Conceptualization (lead); Supervision (equal); Writing – review & editing (equal).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

APPENDIX A: PARAMETERS FOR THE THEORETICAL PREDICTIONS OF THE CONTACT CHARACTERISTICS

The following parameters are employed for the calculations of the GaAs-W and GaAs-Pt metal–semiconductor contact characteristics presented in Table II:

$$N_d(\text{n-GaAs}) = 1 \times 10^{18}\,\text{cm}^{-3},$$

$$N_a(\text{p-GaAs}) = 1 \times 10^{18}\,\text{cm}^{-3},$$

$$N_C(300\ \text{K},\ \text{GaAs}) = 4.45 \times 10^{17}\,\text{cm}^{-3},\ ^{18}$$

$$N_V(300\ \text{K},\ \text{GaAs}) = 9.0 \times 10^{18}\,\text{cm}^{-3},\ ^{18}$$

$$\epsilon_r(\text{GaAs}) = 12.9.^{18}$$

APPENDIX B: HOLOGRAM ACQUISITION PARAMETERS

See Table III for acquisition settings for the *in situ*-biasing electron holography analysis of the GaAs-W and GaAs-Pt specimens.

TABLE III. Acquisition settings for the *in situ*-biasing electron holography analysis of the GaAs-W and GaAs-Pt specimens. The spatial resolution in the phase image results from the mask size applied in the Fourier reconstruction.

Hologram acquisition parameter	GaAs-W	GaAs-Pt
C2 aperture	100 μm	100 μm
Diffraction lens excitation	20%	15%
Lorentz magnification	40.0 kx	40.0 kx
Biprism voltage	80 V	130 V
Pixels per fringe	4	3
Fringe spacing	6.2 nm	3 nm
Spatial resolution (phase image)	18.6 nm	15 nm

APPENDIX C: ELECTRICALLY INACTIVE THICKNESS MEASUREMENT

The procedure for evaluating the electrically inactive thickness is demonstrated by means of the GaAs-W specimen. A prerequisite is preparing a TEM lamella from the bulk semiconductor with regions of different thickness. At each thickness region, the phase shift across the junction is measured using electron holography and STEM-CBED patterns are acquired to measure the crystalline thickness at the junction position. The phase profiles extracted from the phase images for each thickness region of the

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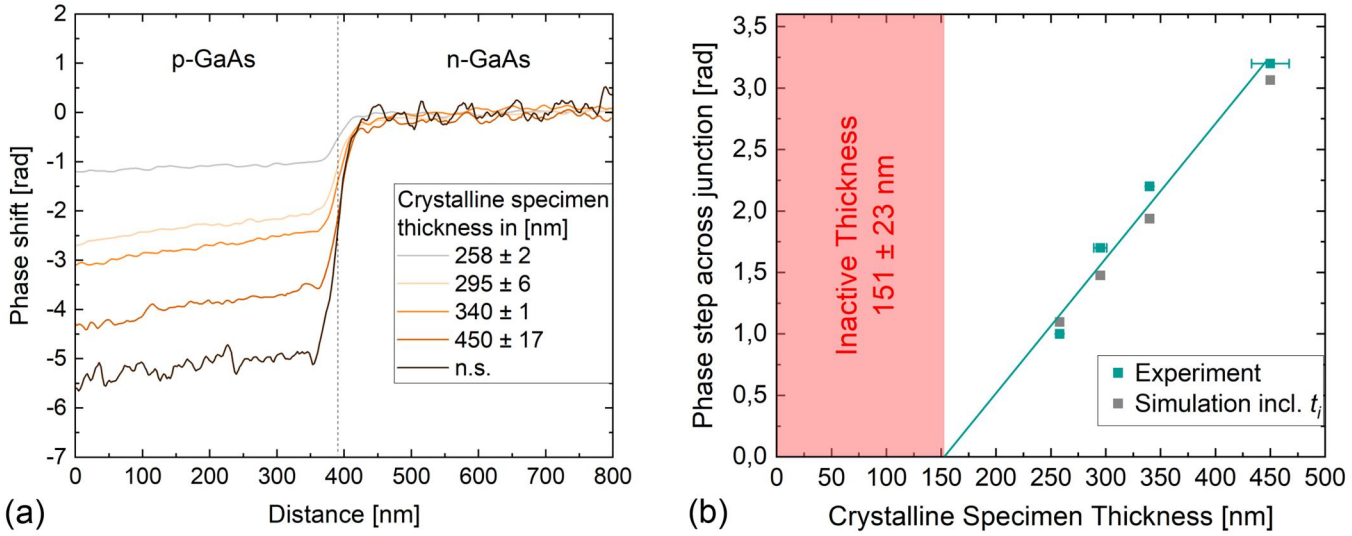


FIG. 6. (a) Phase profiles across the GaAs *p–n* junction extracted from regions of different crystalline thickness of the GaAs-W lamella. (b) Step in electron phase across the *p–n* junction as a function of the total crystalline specimen thickness measured by STEM-CBED. The electrically damaged thickness (t_i) is derived from the x-intercept of the linear fit of the experimental phase values. The expected phase shifts for the remaining electrically active specimen thicknesses, calculated by accounting for the derived t_i, are presented for comparison.

GaAs-W specimen are shown in Fig. 6(a). As expected from Eq. (6), the measured step in phase across the *p–n* junction increases with the specimen thickness. This is also evident from Fig. 6(b), which plots the measured phase steps as a function of the crystalline thickness measured by STEM-CBED. The x-intercept of the linear fit to the experimental data [Fig. 6(b)] indicates the presence of electrically damaged crystalline surface layers. For this GaAs-W specimen, the total thickness of those layers is measured as 151 ± 23 nm. To verify the result, the phase step across the GaAs-W *p–n* junction was simulated for the various electrically active specimen thicknesses t_{active}. The calculation is based on the NEXTNANO simulation of the electrostatic potential of the GaAs *p–n* junction for the given symmetrical doping concentration of 1×10^{18} cm^{-3}.

APPENDIX D: SEPARATION OF THE SCHOTTKY POTENTIAL FROM THE BIAS-INDUCED ELECTRIC FIELD IN p-GaAs

To separate the Schottky-related potential variation from the distributed voltage drop in the p-GaAs layer, the approximately linear potential gradient in the p-GaAs region was fitted and subtracted from each profile, shown in Fig. 7. The fitted gradient increases in magnitude with increasing negative bias [Fig. 7(a)], demonstrating the development of a stronger electric field across the p-GaAs layer. After subtraction of this background contribution [Fig. 7(b)], the potential profiles near the W/p-GaAs interface become nearly bias independent, indicating that the Schottky-related band bending changes only weakly over the investigated voltage range. The increase of the raw potential difference near the contact should, therefore, be attributed mainly to the bias-dependent electric field in the p-GaAs rather than to an increase of the intrinsic Schottky barrier. This interpretation is also consistent with the polarity of the applied bias, since a negative voltage on W corresponds to forward bias of the p-type Schottky contact and tends to increase the hole population near the interface rather than enlarge the depletion region. The apparent depletion extent in the uncorrected profiles remains larger than the 35.6 nm expected from the ideal depletion approximation for $N_A = 10^{18}$ cm^{-3}, further indicating that the raw spatial variation contains both the localized Schottky contribution and the background field. Owing to the increasing oscillations in the potential profiles at larger negative bias, however, the precise depletion width remains subject to substantial experimental uncertainty. This weak variation of the potential step and depletion profile at the W/p-GaAs interface is due to the fact that the W/p-GaAs contact, the p-GaAs layer, and the *p–n* junction form a series-connected structure, and the applied voltage is partitioned among the different resistances. The measured profiles indicate that the *p–n* junction accommodates the largest fraction of the incremental bias, while the Schottky barrier remains comparatively stable, potentially because of the interface electronic structure and Fermi-level pinning. Moreover, owing to the nonlinear *I–V* relation of a Schottky contact, a relatively small change in its local voltage can support a large change in current. The spatially resolved measurement, therefore, provides information that cannot be obtained from terminal *I–V* characteristics alone: it identifies the buried *p–n* junction, rather than the W/p-GaAs interface, as the dominant voltage-sensitive region over the investigated bias range.

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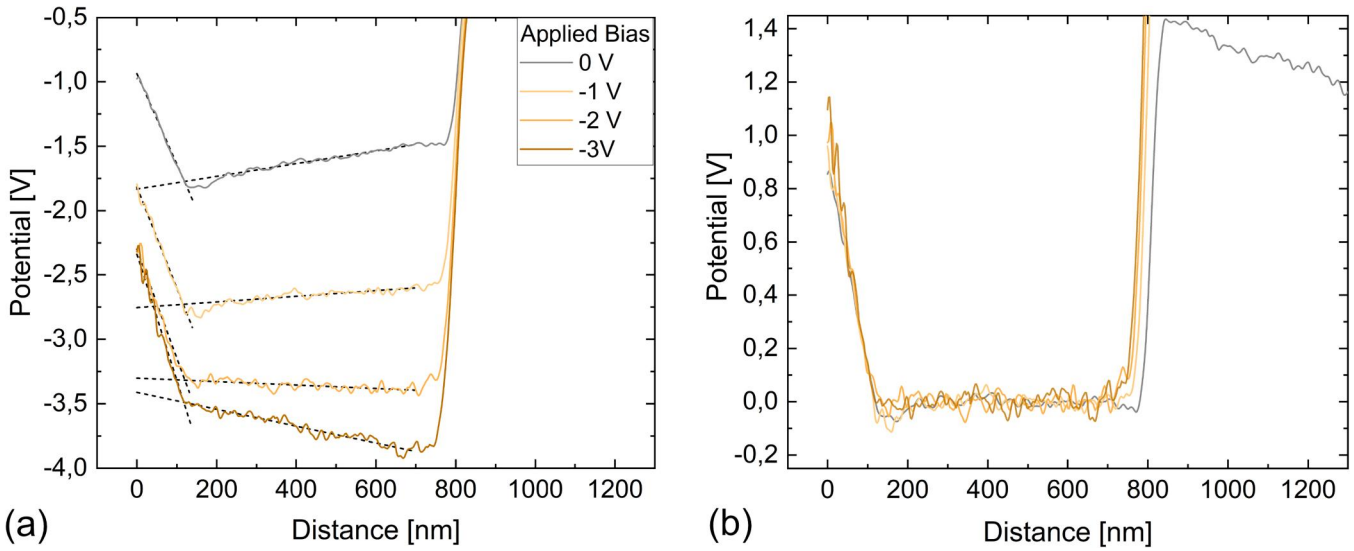


FIG. 7. (a) Potential distributions measured as a function of the applied reverse biases across the GaAs-W specimen as in Fig. 4, here including linear fits to the Schottky W contact depletion region in p-GaAs and the p-GaAs bulk region. (b) The fitted linear potential gradient in the bulk p-GaAs layer was subtracted from the original data in (a).

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