Off-axis electron holography of focused ion beam milled transistors

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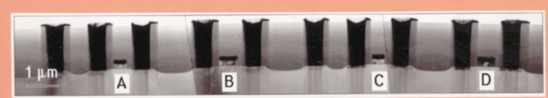
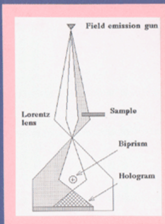
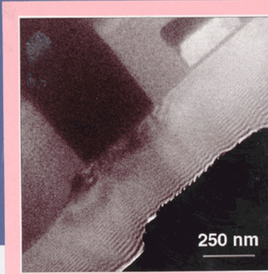
Rau et al. (Phys. Rev. Lett. 82 (1999) 2614) recently used electron holography in the transmission electron microscope (TEM) to map the electrostatic potential in transistors that had been thinned using mechanical polishing and ion milling. *n*- and *p*-type regions were distinguished as bright and dark contrast in phase images, respectively. Here, holography is applied to transistors prepared using focused ion beam milling (FIB), which is widely used to prepare samples in the semiconductor industry.



Bright field image of FIB-prepared sample. A, B, C and D are NMOS (0.35μm gate), NMOS (0.5μm gate), PMOS (0.35μm gate) and PMOS (0.5μm gate) transistors, respectively.

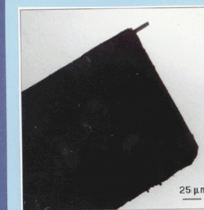
Samples were prepared for TEM examination using FIB. Off-axis electron holograms were recorded at 200 kV in a Philips CM200 field emission gun (FEG) TEM and at 300 kV in a JEOL 3000F FEG TEM. Similar results were obtained using both microscopes.

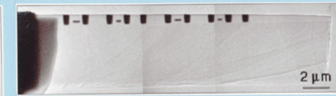




Hologram of PMOS transistor (D in bright field image). 200kV, biprism voltage 160V.

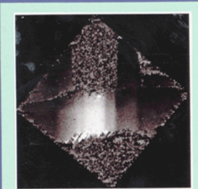
An alternative solution is to perform the final milling from the substrate side. Milling from several directions also allows the very surface of the wafer to be removed, reducing the size of the overlap needed in the hologram between vacuum and the doped region.





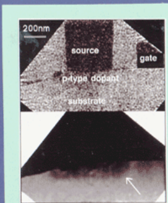
Bright field images of sample milled in several directions using FIB (final thinning from substrate side), with surface subsequently cleaned by low angle milling in a Gatan PIPS.

PROBLEM 1: Focused ion beam milling of a wafer that has a range of compositions on its top surface results in thickness corrugations in the doped region beneath.



Amplitude

Phase

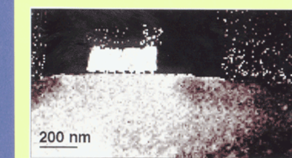


Rapid thickness variations can be seen in the Si substrate, both in the amplitude and particularly in the phase of the reconstructed image wave.

One solution is to determine this (1-D) thickness variation from the region far below the source and drain of the transistor and then to remove the 'corrugation' from the entire sample to leave the depletion region potential of interest.

PROBLEM 2: The majority of semiconductors examined using holography exhibit some form of charging in the TEM, which is often only visible in the reconstructed phase image. Samples were thus coated with a few nm of carbon. Without carbon, rapid variations in phase precluded mapping of the depletion region potential.

PROBLEM 3: Surface depletion creates electrically 'dead' layers on the top and bottom surfaces of a doped sample. Rau et al. (1999) found a thickness for this layer of ~25 nm on each of the two surfaces. A similar analysis here yielded a value of ~50 nm for samples prepared using FIB. A sample of thickness 100 nm therefore exhibited no dopant contrast because the combined thickness of the surface depletion layers was comparable to the total sample thickness.



Phase image obtained from sample of thickness 250 nm after final FIB milling from substrate side, cleaning in a Gatan PIPS and subsequent deposition of a few nm carbon. All of these steps were required to image the depletion region potential in this sample.

CONCLUSION: Off-axis electron holography has been used to examine dopant contrast in transistors prepared for TEM examination using FIB. Artifacts associated with sample thickness variations and charging have been identified, and methods for removing them have been proposed. It should be noted that future work is still required to understand the physics that relates electrostatic potentials measured in semiconductors in the TEM to the forms of the conduction and valence bands.